167 DAC

Docket No.: SON-2352
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tomofumi Arakawa

Application No.: 10/060,226 Confirmation No.: 8077

Filed: February 1, 2002 Art Unit: 2818

For: MEMORY DEVICE Examiner: H. Hoang

PETITION UNDER 37 C.F.R. § 1.181

MS Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant, through its undersigned attorney, hereby petitions to withdraw the holding of abandonment in this case.

The application papers for the above-identified application were deposited with the Patent and Trademark Office (USPTO) on February 1, 2002.

Please accept the application as deposited with the U.S. Patent and Trademark Office on February 1, 2002.

A Notice To File Corrected Application Papers was mailed as the Office letter of **May 2, 2003**. The Notice To File Corrected Application Papers contends that page 12 of the application is missing and that the Applicant must supply the missing information within 30 days of the mail date of the Notice to avoid abandonment. A copy of the Notice To File Corrected Application Papers is provided along with this Petition as ATTACHMENT A.

A Notice of Abandonment was mailed in the above-identified application on **September 24, 2003** as Paper No. 9. The Notice of Abandonment contends that the above-

identified application had become abandoned for failure to timely file a proper reply to the Office letter mailed on May 2, 2003. A copy of the Notice of Abandonment is provided along with this Petition as ATTACHMENT B.

Accordingly, this Petition pursuant to 37 C.F.R. §1.181 is proper.

Evidence

As a timely reply to the Notice To File Corrected Application Papers of May 2, 2003, a Response To Notice To File Corrected Application Papers – Notice Of Allowance Mailed was deposited with the U.S. Patent and Trademark Office (USPTO) on **June 2, 2003**. Please note that June 1, 2003 fell on a Sunday. Since June 2, 2003 is the next day after June 1, 2003 that is neither a Saturday, Sunday nor a Federal holiday, this Response is deemed timely. The Response provides a copy of page 12 and the facsimile dated April 11, 2003. A copy of the Response To Notice To File Corrected Application Papers – Notice Of Allowance Mailed is provided along with this Petition as ATTACHMENT C.

A Part B-Fee(s) Transmittal for payment of the issue fee due and an Amendment Under 37 C.F.R. 1.312(a) After Allowance And Before Payment Of The Issue Fee were filed on **June 10, 2003**. The Amendment Under 37 C.F.R. 1.312(a) submits a substitute specification for entry. A copy of the Part B-Fee(s) Transmittal and the Amendment Under 37 C.F.R. 1.312(a) is provided along with this Petition as ATTACHMENT D.

Notwithstanding the filing on **June 2, 2003** of the Response To Notice To File Corrected Application Papers – Notice Of Allowance Mailed, the Notice of Abandonment was mailed on **September 24, 2003**.

A Request To Withdraw Erroneous Holding Of Abandonment was filed on **October 22, 2003**. A copy of the Request To Withdraw Erroneous Holding Of Abandonment is provided along with this Petition as ATTACHMENT E.

However, the Applicant has no record of receipt of a reply to the Request To Withdraw Erroneous Holding Of Abandonment.

Correspondence address

Also note that the website for the USPTO indicates a Correspondence Address Change in the above-identified application on **October 6, 2003** and indicates yet another Correspondence Address Change in the above-identified application on **April 22, 2004**. The website for the USPTO currently lists Oblon, Spivak, Mcclelland, Maier & Neustadt, P.C., 1940 Duke Street, Alexandria, VA 22314 as the correspondence address of record.

In this regard, please note that the undersigned is unaware of the filing in the above-identified application of a request to change the correspondence address for the above-identified application. As a result, the correct correspondence address for the above-identified application is believed to be the original correspondence address of: Rader, Fishman & Grauer P.L.L.C., 1233 20th Street, N.W., Suite 501, Washington, D.C. 20036.

Relief

Upon this Petition and in view of the evidence submitted, ***withdrawal of the Notice of Abandonment of September 24, 2003*** is respectfully requested.

Upon this Petition and in view of the evidence submitted, correction of the Office records to reflect correspondence address as "Rader, Fishman & Grauer P.L.L.C., 1233 20th Street, N.W., Suite 501, Washington, D.C. 20036" is respectfully requested.

Fee

No fee is believed required to support this Petition. See 37 C.F.R. §1.181.

However, if a fee is required, the Commissioner is hereby authorized to charge the Petition fee to Deposit Account No. 18-0013.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: September 9, 2005

Respectfully submitted,

By _____
Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant

ATTACHMENT A

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

RONALD KANANEN
1233 20TH STREET N W

SUITE 501
WASHINGTON, D C 200036

RKK | NRB 8000-2352

Serial No.: 10/060226
Applicant: ARAKAWA, TOMOFUMI
Filing Date: 02/01/2002
Date Mailed: 05/02/2003

June 1, 2003

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 30 days from the mail date of this Notice within which to correct the informalities indicated below. A failure to reply will result in the application being ABANDONED. This period for reply is NOT extendable under 37 CFR 1.136 (a) or (b).

Page 12 is missing.

APPLICANT MUST SUPPLY MISSING INFORMATION WITHIN 30 DAYS OF THE MAIL DATE OF THIS NOTICE.

A copy of this notice MUST be returned with the reply. Please address response to "Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313"

David Irvine

Name: David Irvine
Data Query
Phone 703-305-8391
Fax 703-308-6642

ATTACHMENT B

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,226	02/01/2002	Tomofumi Arakawa	SON-2352	8077

23353 7590 09/24/2003

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/24/2003

SON 8077-2352

pet to revive
Oct 24, 2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Abandonment

Application No.	Applicant(s)	
10/060,226	ARAKAWA, TOMOFUMI	
Examiner	Art Unit	
Huan Hoang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *02 May 2003*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☐ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☒ The reason(s) below:

Page 12 of the specificaiton is missing.

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

ATTACHMENT C

Atty Docket No.: SON-2352

Inventor: Tomofumi Arakawa

Application No.: 10/060,226 **Filing Date:** February 1, 2002
Title: MEMORY DEVICE

Documents Filed:
Response to Notice to File Corrected Application Papers

Via:
Sender's Initials: RPK/sjm **Date:** June 2, 2003

SON-2352 ATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Tomofumi Arakawa

Application No.: 10/060,226 Group Art Unit: 2818

Filed: February 1, 2002 Examiner: Huan Hoang

For MEMORY DEVICE

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS - NOTICE OF ALLOWANCE MAILED

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Corrected Application Papers mailed May 2, 2003 (copy of which is returned herewith), applicants hereby submit a copy of page 12 of the specification for the above-identified application.

It may be noted that the alleged missing page 12 was forwarded by facsimile on April 11, 2003.

Should there be any questions regarding the application, the Examiner is invited to telephone the undersigned at telephone number listed below.

No fees are believed to be required. However, the Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 18-0013. A duplicate copy of this letter is enclosed for that purpose.

Respectfully submitted,

DATE: June 2, 2003

Ronald P. Kananen
Reg. No. 24,104

RADER, FISHMAN & GRAUER PLLC
Lion Building
1233 20th Street, N.W.
Washington, D.C. 20036
Tel: (202) 955-3750

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

RONALD KANANEN
1233 20TH STREET N W

SUITE 501
WASHINGTON, D C 200036

NAL/NRB 80001-2352

Serial No. : 10/060226
Applicant : ARAKAWA, TOMOFUMI
Filing Date : 02/01/2002
Date Mailed : 05/02/2003

June 1, 2003

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 30 days from the mail date of this Notice within which to correct the informalities indicated below. A failure to reply will result in the application being ABANDONED. This period for reply is NOT extendable under 37 CFR 1.136 (a) or (b).

Page 12 is missing.

APPLICANT MUST SUPPLY MISSING INFORMATION WITHIN 30 DAYS OF THE MAIL DATE OF THIS NOTICE.

A copy of this notice MUST be returned with the reply. Please address response to "Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313"

David Irvine

Name : David Irvine
Data Query
Phone 703-305-8391.
Fax 703-308-6642

1233 20th Street
Suite 501
Washington, D.C. 20036
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Facsimile (202) 955-3751
http://www.intelprop.com
info@raderfishman.com

RADER, FISHMAN & GRAUER PLLC

Fax

To: DAVID RUNP - Relay Assist **From:** R.P. Cranen

Fax: 703/308-6642 **Pages:** 1 (including this cover page)

Phone: **Date:** 4/11/03

Re:

CC:

☐ **Urgent** ☐ **For Review** ☐ **Please Comment** ☐ **Please Reply** ☐ **Please Recycle**

SON-2352

• **Comments:**

RE: Serial # 10/060,226
page 12 as requested from the specification

DC014800

controls the memory device shown in FIG. 3. Address represents row and column address signals from the microcomputer. WL0 and WL1 represent the respective high and low voltages of the word lines WL0 and WL1, respectively. SA0-0, SA0-1, ..., and SA0-n represent the respective voltages of the sense amplifiers 30A-0, 30A-1, ..., and 30A-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively. SA1-0, SA1-1, ..., and SA1-n represent the respective voltages of the sense amplifiers 30B-0, 30B-1, ..., and 30B-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively.

Data Out represents output data outputted to the read data bus through the read gates. Data In represents input data supplied from the write data bus to the write gates. TGSel represents a gate select signal indicative of either the transfer gate 20A or 20B, from the microcomputer. TG0 and TG1 represent the control signals supplied to the transfer gates 20A and 20B, respectively.

The command Command first indicates ACT to a row address RA0 so as to activate the row address RA0, thus the word line WL0 first changes from low level to high level, and thus the command Command changes to Read so as to read column addresses CA00 and CA01. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the sense amplifiers 30A-0 and 30A-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Then, the sense amplifiers 30A-0 and 30A-1 output the amplified data

ATTACHMENT D

Atty Docket No.: SON-2352

Inventor: Tomofumi Arakawa

Application No.: 10/060,226 **Filing Date:** February 1, 2002
Title: MEMORY DEVICE

Documents Filed:
Issue Fee

312 Amendment/Substitute Specification/Red-Lined

Via:
Sender's Initials: RPK/sjm **Date:** June 10, 2003

PART B - FEE(S) TRANSMITTAL

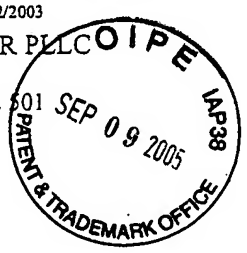
Complete and send this form, together with applicable fee(s), to: Mail **Box ISSUE FEE**
Commissioner for Patents
Washington, D.C. 20231
Fax **(703)746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

23353 7590 03/12/2003

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,226	02/01/2002	Tomofumi Arakawa	SON-2352	8077

TITLE OF INVENTION: MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1300	$300	$1600	06/12/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2818	365-149000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Rader, Fishman & Grauer PLLC
2 Ronald P. Kananen
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Sony Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

☒ Issue Fee
☒ Publication Fee
☒ Advance Order - # of Copies 3

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 18-0013 (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date) 6/10/03

Ronald P. Kananen, Reg. No. 24,104

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

SON-2352

BOX ISSUE FEE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Tomofumi Arakawa

Application No.: 10/060,226

Filed: February 1, 2002

For: MEMORY DEVICE

Confirmation No. 8077

Group Art Unit: 2818

Examiner: Huan Hoang

AMENDMENT UNDER 37 C.F.R. 1.312(a) AFTER ALLOWANCE AND BEFORE PAYMENT OF THE ISSUE FEE

Commissioner for Patents
Mail Stop Issue Fee
P.O. Box 1450
Alexandria, Va 22313-1450

Sir:

Subsequent to the Notice of Allowance of March 12, 2003, but before payment of the issue fee, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the application by entering the enclosed substitute specification in place of that which was previously filed. A red-lined version is also attached.

IN THE CLAIMS:

Please amend the claims as set forth below in marked-up version. The claims have been amended to attend to grammatical and typographical errors. As set forth in the new amendment format, a clean version of the amended claims is not required.

1. (Amended) A memory device comprising:

a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines;

a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and

a read gate and a write gate ~~which~~ that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines,

wherein the memory device is controlled so that read data ~~is~~ are read out successively~~,~~ when a word line to be activated~~,~~ of the plurality of word lines is switched to another word line to be activated.

2. (Amended) The memory device according to claim 1 comprising a plurality of read gates and a plurality of write gates ~~which~~ that are separately connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

3. (Amended) The memory device according to claim 1 comprising a common read gate and a common write gate ~~which~~ that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

4. (Original) The memory device according to claim 1, wherein each of the plurality of memory cells comprises a dynamic RAM.

5. (Original) The memory device according to claim 2, wherein each of the plurality of memory cells comprises a dynamic RAM.

6. (Original) The memory device according to claim 3, wherein each of the plurality of memory cells comprises a dynamic RAM.

REMARKS

This is a 312 Amendment after allowance and before payment of the issue fee to correct grammatical errors and readability in the specification. No new matter has been added.

Respectfully submitted,

Dated: June 10, 2003

Ronald P. Kananen
Reg. No. 24,104

RADER, FISHMAN & GRAUER PLLC
1233 20TH Street, NW
Suite 501
Washington, DC 20036
Telephone:(202) 955-3750
Facsimile: (202) 955-3751
Customer No. 23353

MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a memory device.

Description of the Related Art

A D-RAM (dynamic random access memory) of the prior art will be described below with reference to FIG. 1 and FIG. 2 specifically showing some of circuits shown in FIG. 1. The D-RAM has: plural, (n+1) pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; plural, (m+1) word lines WL0, WL1, ..., and WLm which intersect the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; a matrix of a plurality of D-RAM memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n}, each of which is connected to an intersection of each bit line and each word line; and sense amplifiers 30-0, 30-1, ..., and 30-n connected to the memory cells 10-0, 10-1, ..., and 10-n, each of which comprises a plurality of memory cells, through the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively.

Each of the memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n} comprises, for example, an N-channel (or P-channel) type MOS-FET Q, which functions as a switching transistor, and a capacitor C connected in series with the MOS-FET Q.

The drains of the MOS-FETs Q of the memory cells MC0-0, MC2-0, MC4-0, ... of the memory cell 10-0, the memory cells MC0-1, MC2-1, MC4-1, ... of the memory cell 10-1, ..., and the

memory cells MC0-n, MC2-n, MC4-n, ... of the memory cell 10-n are connected to the bit lines BL0, BL1, BL2, ..., and BLn, the gates thereof are connected to the word lines WL0, WL2, WL4, ..., and the sources thereof are connected to cell plate potential lines VL to which a common cell plate potential Vcp is applied, through the capacitors C.

The drains of the MOS-FETs Q of the memory cells MC1-0, MC3-0, MC5-0, ... of the memory cell 10-0, the memory cells MC1-1, MC3-1, MC5-1, ... of the memory cell 10-1, ..., and the memory cells MC1-n, MC3-n, MC5-n, ... of the memory cell 10-n are connected to the bit lines BLB0, BLB1, BLB2, ..., and BLBn, the gates thereof are connected to the word lines WL1, WL3, WL5, ..., and the sources thereof are connected to the cell plate potential lines VL to which the common cell plate potential Vcp is applied, through the capacitors C.

Each of the sense amplifiers 30-0, 30-1, ..., and 30-n comprises P-channel type MOS-FETs Q1 and Q2 that are connected in series between the bit lines BL0 and BLB0, between the bit lines BL1 and BLB1, ..., and between the bit lines BLn and BLBn and whose gates are connected to the bit lines BLB0, BLB1, ..., BLBn and the bit lines BL0, BL1, ..., and BLn, respectively,and N-channel type MOS-FETs Q3 and Q4 that are connected in series between the bit lines BL0 and BLB0, between the bit lines BL1 and BLB1, ..., and between the bit lines BLn and BLBn and whose gates are connected to the bit lines BLB0, BLB1, ..., BLBn and the bit lines BL0, BL1, ..., and BLn, respectively. Each sense amplifier is configured so that a driving signal from a sense amplifier driver is supplied to the midpoint of connection between the P-channel type MOS-FETs Q1 and Q2 and the midpoint of connection between the N-channel type MOS-FETs Q3 and Q4.

Data read out from the memory cells 10-0, 10-1, ..., and 10-m, each of which comprises a plurality of memory cells, are

transmitted to a read DB (data bus) through the sense amplifiers 30-0, 30-1, ..., and 30-n and read gates 40-0, 40-1, ..., and 40-n. Data from a write DB (data bus) are transmitted to and written in the memory cells 10-0, 10-1, ..., and 10-m through write gates 50-0, 50-1, ..., and 50-n and the sense amplifiers 30-0, 30-1, ..., and 30-n.

A D-RAM of the prior art shown in FIG. 3 comprises the D-RAM shown in FIG. 1, and additional read gates 41-0, 41-1, ..., and 41-n that are provided for the sense amplifiers 30-0, 30-1, ..., and 30-n, respectively. When a transfer gate 20 is on, data read out from the memory cells 10-0, 10-1, ..., and 10-m, each of which comprises a plurality of memory cells, are transmitted to the read DB (data bus) through the sense amplifiers 30-0, 30-1, ..., and 30-n, the transfer gate 20, D latches 60-0, 60-1, ..., and 60-n and the read gates 41-0, 41-1, ..., and 41-n. When the transfer gate 20 is off, the memory device shown in FIG. 3 operates in the same manner as the memory device shown in FIG. 1. The other configuration of the memory device is the same as that of the memory device shown in FIG. 1.

The D-RAM of the prior art shown in FIG. 3 has the following problem. Since data read out from the memory cells 10-0, 10-1, ..., and 10-m pass through the sense amplifiers 30-0, 30-1, ..., and 30-n when the data are transmitted to the D latches 60-0, 60-1, ..., and 60-n, this makes it impossible to make access to the sense amplifiers 30-0, 30-1, ..., and 30-n during the passage of the data or the read data overwrite data of the sense amplifiers 30-0, 30-1, ..., and 30-n.

The above-mentioned D-RAM has a problem of a long access time to a row line. This results from the fact that data of the memory cells of the D-RAM must be amplified and latched by the sense amplifiers before the data are read out. This is a fundamental problem of the D-RAM.

In order to solve the above-mentioned problems, a plurality of D-RAMs or a D-RAM having a bank structure is used so that the D-RAM operates using banks. More specifically, when access to a bank is being made, another bank is activated to previously enter a ready state so that data are read out consecutively. This is called interleaving. This allows apparently hiding the setup time (tRCD) and the reset time (tPR) required for the D-RAM.

It is possible that a plurality of D-RAMs or the D-RAM having the bank structure is used in order that the D-RAM having a conventional configuration may realize the operation using banks. When a plurality of D-RAMs is used, each D-RAM is not good in area efficiency, but each D-RAM is not limited in operation. On the other hand, the D-RAM having the bank structure is good in area efficiency, because a part of a circuit is common among banks, whereas each bank is partly limited in operation.

The D-RAM has the properties that its larger storage capacity yields its higher area efficiency, while its smaller storage capacity yields its lower area efficiency, similarly to other types of memories. A D-RAM having a multibank structure causes a reduction in area efficiency. Assume that a mixed D-RAM comprises banks of varying minimum units (i.e., blocks), e.g., a 2-Mbit block, a 1-Mbit block, and a 512-Kbit block. If a 4-Mbit D-RAM is manufactured without consideration of the bank structure, the decreasing order of area efficiency, from highest to lowest, is the 2-Mbit block, the 1-Mbit block, and the 512-Kbit block. When a 4-Mbit D-RAM is manufactured in consideration of the bank structure, the D-RAM can be, however, occupied by up to two banks each having the 2-Mbit block, up to four banks each having the 1-Mbit block, or up to eight banks each having the 512-Kbit block. Even if a D-RAM comprises two

banks each having the 1-Mbit or 512-Kbit block, the area efficiency of the D-RAM is not different from that of a D-RAM comprising four banks each having the 1-Mbit block or eight banks each having the 512-Kbit block.

However, a D-RAM having a larger capacity than the necessary capacity, if a small-capacity D-RAM is used, must be used in order that the D-RAM may operate using banks. In terms of area efficiency, the reason is that the size of the block that is the minimum unit of the bank is large. For example, when a user wants to use a 1-Mbit D-RAM in the form of two banks, a D-RAM of at least 2 Mbits must be used to obtain a D-RAM having a two-bank structure, provided that one block equals 1 Mbit.

The above-mentioned D-RAM adopts a bank method in order to apparently hide the access time to a row line requiring consecutive data.

However, the bank method has to be provided with a D-RAM macro (which refers to a group of circuits having the functions of a D-RAM), and therefore the method is often disadvantageous in area to an application that needs only a small capacity.

A RAM having a capacity of at least 2 Mbits or more must be packaged to employ a bank structure for, for example, an application that requires a RAM having a capacity of only 1 Mbit, if a macro size that can be provided is 1 Mbit and the use of a plural-bank structure is demanded.

The invention is designed to overcome the foregoing problems. It is an object of the invention to provide a memory device which can minimize a reduction in area efficiency, even when the memory device has a small storage capacity, and which can hide the access time to a row line.

SUMMARY OF THE INVENTION

According to a first aspect of the invention, there is provided a memory device which comprises: a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines; a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and a read gate and a write gate that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, wherein the memory device is controlled so that read data are read out successively when a word line to be activated of the plurality of word lines is switched to another word line to be activated.

According to the first aspect of the invention, a plurality of memory cells is arranged in a matrix in such a manner that each memory cell is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines, a plurality of sense amplifiers capable of read and write operations independently of one another is disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines, a read gate and a write gate are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, and the memory device is controlled so that read data are read out successively when a word line to be activated of the plurality of word lines is switched to another word line to be activated.

According to a second aspect of the invention, there is provided the memory device of the first aspect which comprises a

plurality of read gates and a plurality of write gates that are separately connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to a third aspect of the invention, there is provided the memory device of the first aspect which comprises a common read gate and a common write gate that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to fourth, fifth and sixth aspects of the invention, there are provided the memories of the first, second and third aspects, wherein each of the plurality of memory cells comprises a dynamic RAM.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a conventional D-RAM;

FIG. 2 is a circuit diagram specifically showing some of circuits shown in FIG. 1;

FIG. 3 is a block diagram showing another conventional D-RAM;

FIG. 4 is a block diagram showing an example of a memory device according to an embodiment of the invention;

FIG. 5 is a timing chart showing waveforms for use in the description of operation of the memory device shown in FIG. 4;

FIG. 6 is a block diagram showing another example of the memory device according to the embodiment of the invention;

FIG. 7 is a timing chart showing waveforms for use in the description of operation of the memory device shown in FIG. 6; and

FIG. 8 is a timing chart showing waveforms for use in the description of operation of the memory devices shown in FIGS. 4 and 6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An example of a memory device (a D-RAM) according to an embodiment of the invention will be described below with reference to FIG. 4. Memory cells 10-0, 10-1, ..., and 10-n each comprise a plurality of memory cells, each of which is connected to the intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines, similarly to the memory cells described with reference to FIG. 2.

More specifically, the D-RAM has plural, (n+1) pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; plural, (m+1) word lines WL0, WL1, ..., and WLm which intersect the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; a matrix of a plurality of D-RAM memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n}, each of which is connected to an intersection of each bit line and each word line; and a plurality of sense amplifiers 30A-0, 30A-1, ..., and 30A-n, and 30B-0, 30B-1, ..., and 30B-n capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the memory cells 10-0, 10-1, ..., and 10-n, each of which comprises a plurality of memory cells, through the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn via transfer gates 20A and 20B that are turned on and off in accordance with gate signals TG0 and TG1, respectively.

The configuration of the sense amplifiers 30A-0, 30A-1, ..., and 30A-n, and 30B-0, 30B-1, ..., and 30B-n is the same as that of the sense amplifiers described above with reference to FIG. 2.

Each of the memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n} comprises, for example, an N-channel (or P-channel) type MOS-FET Q, which functions as a switching transistor, and a capacitor C connected in series with the MOS-FET Q.

The drains of the MOS-FETs Q of the memory cells MC0-0, MC2-0, MC4-0, ... of the memory cell 10-0, the memory cells MC0-1, MC2-1, MC4-1, ... of the memory cell 10-1, ..., and the memory cells MC0-n, MC2-n, MC4-n, ... of the memory cell 10-n are connected to the bit lines BL0, BL1, BL2, ..., and BLn, the gates thereof are connected to the word lines WL0, WL2, WL4, ..., and the sources thereof are connected to cell plate potential lines VL to which a common cell plate potential Vcp is applied, through the capacitors C.

The drains of the MOS-FETs Q of the memory cells MC1-0, MC3-0, MC5-0, ... of the memory cell 10-0, the memory cells MC1-1, MC3-1, MC5-1, ... of the memory cell 10-1, ..., and the memory cells MC1-n, MC3-n, MC5-n, ... of the memory cell 10-n are connected to the bit lines BLB0, BLB1, BLB2, ..., and BLBn, the gates thereof are connected to the word lines WL1, WL3, WL5, ..., and the sources thereof are connected to the cell plate potential lines VL to which the common cell plate potential Vcp is applied, through the capacitors C.

Read gates 40A-0, 40A-1, ..., and 40A-n and write gates 50A-0, 50A-1, ..., and 50A-n are connected to the sense amplifiers 30A-0, 30A-1, ..., and 30A-n, respectively.

Read gates 40B-0, 40B-1, ..., and 40B-n and write gates 50B-0, 50B-1, ..., and 50B-n are connected to the sense amplifiers 30B-0, 30B-1, ..., and 30B-n, respectively.

Data read out from the memory cells 10-0, 10-1, ..., and 10-m are transmitted to a read DB (data bus) through the transfer gate 20A, which is turned on in accordance with the gate control signal TG0, the sense amplifiers 30A-0, 30A-1, ..., and 30A-n and the read gates 40A-0, 40A-1, ..., and 40A-n, or through the transfer gate 20B, which is turned on in accordance with the gate control signal TG1, the sense amplifiers 30B-0, 30B-1, ..., and 30B-n and the read gates 40B-0, 40B-1, ..., and 40B-n.

Data from a write DB (data bus) are transmitted to and written in the memory cells 10-0, 10-1, ..., and 10-n through the write gates 50A-0, 50A-1, ..., and 50A-n, the sense amplifiers 30A-0, 30A-1, ..., and 30A-n and the transfer gate 20A turned on in accordance with the gate control signal TG0, or through the write gates 50B-0, 50B-1, ..., and 50B-n, the sense amplifiers 30B-0, 30B-1, ..., and 30B-n and the transfer gate 20B turned on in accordance with the control signal TG1.

Next, the operation of the memory device shown in FIG. 4 will be described with reference to a timing chart shown in FIG. 5. In FIG. 5, CLK represents a clock waveform. Command represents a command from a microcomputer (not shown) which controls the memory device shown in FIG. 3. Address represents row and column address signals from the microcomputer. WL0 and WL1 represent the respective high and low voltages of the word lines WL0 and WL1, respectively. SA0_0, SA0_1, ..., and SA0_n represent the respective voltages of the sense amplifiers 30A-0, 30A-1, ..., and 30A-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively. SA1_0, SA1_1, ..., and SA1_n represent the respective voltages of the sense amplifiers 30B-0, 30B-1, ..., and 30B-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively.

Data Out represents output data outputted to the read data bus through the read gates. Data In represents input data supplied from the write data bus to the write gates. TGSel represents a gate select signal indicative of either the transfer gate 20A or 20B, from the microcomputer. TG0 and TG1 represent the control signals supplied to the transfer gates 20A and 20B, respectively.

The command Command first indicates ACT to a row address RA0 so as to activate the row address RA0, thus the word line WL0 first changes from low level to high level, and thus the command Command changes to Read so as to read column addresses CA00 and CA01. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the sense amplifiers 30A-0 and 30A-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Then, the sense amplifiers 30A-0 and 30A-1 output the amplified data is transmitted as output data Q00 and Q01 to the read data bus through the read gates 40A-0 and 40A-1, respectively.

The command Command then indicates ACT so as to activate a row address RA1, and thus the word line WL1 first changes from low level to high level so as to read out data of the memory cells. Then, the data are amplified, and thereafter the command Command changes to Read so as to read column addresses CA10 and CA11. After that, the gate select signal TGSel changes to TG1 so as to change the gate signal TG1 from low level to high level, and thus the transfer gate 20B is turned on so as to allow the sense amplifiers 30B-0 and 30B-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Then, the sense amplifiers 30B-0 and 30B-1 output the amplified data as output data Q10 and Q11 to the read data bus through the read gates 40B-0 and 40B-1, respectively.

The command Command changes to Write, thus the column addresses CA00 and CA01 are read, and data D00 and D01 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30A-0 and 30A-1 through the write gates 50A-0 and 50A-1, respectively. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30A-0 and 30A-1, respectively.

In a state in which the command Command remains Write, the column addresses CA10 and CA11 are read, and data D10 and D11 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30B-0 and 30B-1 through the write gates 50B-0 and 50B-1, respectively. After that, the gate select signal TGSel changes to TG1 so as to change the gate signal TG1 from low level to high level, and thus the transfer gate 20B is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30B-0 and 30B-1, respectively.

After that, the command Command changes to PRE (precharge) so as to precharge the bit lines BL1 and BLB1 of the row address RA1, and thus an equal constant voltage is applied to the bit lines BL1 and BLB1.

Another example of the memory device according to the embodiment of the invention will be described below with reference to FIG. 6. In FIG. 6, the parts corresponding to the parts shown in FIG. 4 are indicated by the same reference numerals and characters, and the description of these parts is omitted to avoid repetition. Similarly to the memory device shown in FIG. 4, the memory device shown in FIG. 6 has plural, (n+1) pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and

BLn and BLBnplural, (m+1) word lines WL0, WL1, ..., and WLm which intersect the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; a matrix of a plurality of D-RAM memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n}, each of which is connected to an intersection of each bit line and each word line; and a plurality of sense amplifiers 30A-0, 30A-1, ..., and 30A-n, and 30B-0, 30B-1, ..., and 30B-n capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the memory cells 10-0, 10-1, ..., and 10-n, each of which comprises a plurality of memory cells, through the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn via transfer gates 20A and 20B that are turned on and off in accordance with gate signals TG0 and TG1, respectively.

In this example, common read gates 40-0, 40-1, ..., and 40-n and common write gates 50-0, 50-1, ..., and 50-n are connected in parallel with the sense amplifiers 30A-0 and 30B-0, 30A-1 and 30B-1, ..., and 30A-n and 30B-n through transfer gates 20C and 20D that are turned on and off in accordance with gate signals TGA0 and TGA1, respectively. The other configuration of the memory device shown in FIG. 6 is the same as that of the memory device shown in FIG. 4.

Next, the operation of the memory device shown in FIG. 6 will be described with reference to a timing chart shown in FIG. 7. In FIG. 7, the parts corresponding to the parts shown in FIG. 5 are indicated by the same reference numerals and characters, and thus the description of these parts is omitted to avoid repetition. TGASel represents a gate select signal indicative of either the transfer gate 20C or 20D.

The command Command first indicates ACT so as to activate a row address RA0; thus, the word line WL0 first changes from low level to high level, the command Command changes to Read, and the gate select signal TGSel changes to TG0 so as to read column addresses CA00 and CA01. After that, the gate signal TG0 changes from low level to high level, and thus the transfer gate 20A is turned on so as to allow the sense amplifiers 30A-0 and 30A-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Thereafter, the gate select signal TGASel changes to TGA0 so as to change the gate signal TGA0 from low level to high level, and thus the transfer gate 20C is turned on. Then, the sense amplifiers 30A-0 and 30A-1 output the amplified data as output data Q00 and Q01 to the read data bus through the read gates 40-0 and 40-1, respectively.

The command Command then indicates ACT so as to activate a row address RA1; thus, the word line WL1 first changes from low level to high level, the command Command changes to Read, and the gate select signal TGSel changes to TG1 so as to read column addresses CA10 and CA11. After that, the gate signal TG1 changes from low level to high level, and thus the transfer gate 20B is turned on so as to allow the sense amplifiers 30B-0 and 30B-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Thereafter, the gate select signal TGASel changes to TGA1 so as to change the gate signal TGA1 from low level to high level, and thus the transfer gate 20D is turned on. Then, the sense amplifiers 30B-0 and 30B-1 output the amplified data as output data Q10 and Q11 to the read data bus through the read gates 40-0 and 40-1, respectively.

The command Command changes to Write, and thus the column addresses CA00 and CA01 are read. The gate select signal TGASel first indicates TGA0 so as to change the gate signal TGA0 from low level to high level, and thus the transfer gate 20C is

turned on. Data D00 and D01 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30A-0 and 30A-1 through the write gates 50-0 and 50-1, respectively. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30A-0 and 30A-1, respectively.

In a state in which the command Command remains Write, the column addresses CA10 and CA11 are read. The gate select signal TGASel first indicates TGA1 so as to change the gate signal TGA1 from low level to high level, and thus the transfer gate 20D is turned on. Data D10 and D11 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30B-0 and 30B-1 through the write gates 50-0 and 50-1, respectively. After that, the gate select signal TGSel changes to TG1 so as to change the gate signal TG1 from low level to high level, and thus the transfer gate 20B is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30B-0 and 30B-1, respectively.

After that, the command Command changes to PRE (precharge) so as to precharge the bit lines BL1 and BLB1 of the row address RA1, and thus an equal constant voltage is applied to the bit lines BL1 and BLB1.

Incidentally, a D-RAM is characterized by the activation of an address of a row line allows a sense amplifier to read out a few thousands of bits of data, which is then selectively read out by controlling an address of a column line. Generally, the operation of activating the address of the row line so as to prepare data for reading is very slow, which is a drawback of the D-RAM. The technique for eliminating the drawback is interleaving using a bank structure, which is described in the

section "Description of the Related Art". More specifically, when data of a bank are being read out, data of another bank are prepared, and thus the latter data can be read out in succession to the former data immediately after the end of reading the former data. However, the interleaving requires a plurality of banks, and therefore causes a reduction in area efficiency in the case of a small-capacity memory device.

However, the memories shown in FIGS. 4 and 6 are each provided with a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with a plurality of memory cells, each of which is connected to each of the pairs of bit lines, through the pairs of bit lines, and the memories are controlled so that read data may be read out successively when a word line to be activated of a plurality of word lines is switched to another word line to be activated. Therefore, the above-described memories can minimize the reduction in area efficiency even when the memories have a small capacity, and the memories also enable operation equivalent to the interleaving performed by a memory device having a bank structure (see FIG. 8).

In FIG. 8, the parts corresponding to the parts shown in FIGS. 5 and 7 are indicated by the same reference numerals and characters, and thus the description of these parts is omitted to avoid repetition.

The memories shown in FIGS. 4 and 6 are each provided with a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with a plurality of memory cells, each of which is connected to each of the pairs of bit lines, through the pairs of bit lines, and read gates and write gates that are connected to a plurality of sense amplifiers

connected to a plurality of memory cells. Therefore, when one sense amplifier is being used to write and read data in/from a memory cell, another sense amplifier can be used to sense a subsequent row address, so that an erroneous hit of a page can be prevented.

When one sense amplifier is being used to write and read data in/from a memory cell, another sense amplifier may be used as a static RAM (an S-RAM).

For example, when 2-Mbit blocks are used to manufacture a D-RAM having a storage capacity of 4 Mbits, the D-RAM has a structure of only up to two banks. Therefore, 1-Mbit or 512-Kbit blocks must be used in order that a D-RAM may comprise four banks. However, as described above, the adoption of a system comprising a plurality of sense amplifiers permits manufacturing a D-RAM having functions substantially equivalent to functions of a D-RAM comprising four banks using 2-Mbit blocks. Accordingly, although a larger number of additional sense amplifiers yield a lower area efficiency of a memory device, the memory device is greatly improved in area efficiency as compared to a memory device using 1-Mbit or 512-Kbit blocks.

According to a first aspect of the invention, a memory device comprises: a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines; a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and a read gate and a write gate that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, wherein the memory

device is controlled so that read data are read out successively, when a word line to be activated, of the plurality of word lines is switched to another word line to be activated. Therefore, the memory device can minimize a reduction in area efficiency, even when the memory device has a small storage capacity, realize operation equivalent to interleaving using the bank structure, hide the access time to a row line, and can use as an S-RAM any one of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to a second aspect of the invention, the memory device of the first aspect comprises a plurality of read gates and a plurality of write gates that are separately connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines. Therefore, the memory device can minimize the reduction in area efficiency even when the memory device has a small storage capacity, realize operation equivalent to interleaving using the bank structure, hide the access time to a row line, and use as an S-RAM any one of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to a third aspect of the invention, the memory device of the first aspect comprises a common read gate and a common write gate that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines. Therefore, the memory device can minimize a reduction in area efficiency, even when the memory device has a small storage capacity, realize operation equivalent to interleaving using the bank structure, hide the access time to a row line, use as an S-RAM any one of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, and have a smaller number of read gates and write gates connected to the plurality of

sense amplifiers connected in parallel with the pairs of bit lines.

In the memories of the first, second and third aspects, each of the plurality of memory cells comprises a dynamic RAM.

Having described preferred embodiments of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments and that various changes and modifications could be effected therein by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended claims.

ABSTRACT OF THE DISCLOSURE

Disclosed is a memory device which can minimize a reduction in area efficiency even when the memory device has a small storage capacity and which can hide the access time to a row line. The memory device comprises: a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines; a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and a read gate and a write gate which are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, wherein the memory device is controlled so that read data are read out successively when a word line to be activated of the plurality of word lines is switched to another word line to be activated.

MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a memory device.

Description of the Related Art

A D-RAM (dynamic random access memory) of the prior art will be described below with reference to FIG. 1 and FIG. 2 specifically showing some of circuits shown in FIG. 1. The D-RAM has: plural, (n+1) pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; plural, (m+1) word lines WL0, WL1, ..., and WLm which intersect the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; a matrix of a plurality of D-RAM memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n}, each of which is connected to an intersection of each bit line and each word line; and sense amplifiers 30-0, 30-1, ..., and 30-n connected to the memory cells 10-0, 10-1, ..., and 10-n, each of which comprises a plurality of memory cells, through the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively.

Each of the memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n} comprises, for example, an N-channel (or P-channel) type MOS-FET Q, which functions as a switching transistor, and a capacitor C connected in series with the MOS-FET Q.

The drains of the MOS-FETs Q of the memory cells MC0-0, MC2-0, MC4-0, ... of the memory cell 10-0, the memory cells MC0-1, MC2-1, MC4-1, ... of the memory cell 10-1, ..., and the

memory cells MC0-n, MC2-n, MC4-n, ... of the memory cell 10-n are connected to the bit lines BL0, BL1, BL2, ..., and BLn, the gates thereof are connected to the word lines WL0, WL2, WL4, ..., and the sources thereof are connected to cell plate potential lines VL to which a common cell plate potential Vcp is applied, through the capacitors C.

The drains of the MOS-FETs Q of the memory cells MC1-0, MC3-0, MC5-0, ... of the memory cell 10-0, the memory cells MC1-1, MC3-1, MC5-1, ... of the memory cell 10-1, ..., and the memory cells MC1-n, MC3-n, MC5-n, ... of the memory cell 10-n are connected to the bit lines BLB0, BLB1, BLB2, ..., and BLBn, the gates thereof are connected to the word lines WL1, WL3, WL5, ..., and the sources thereof are connected to the cell plate potential lines VL to which the common cell plate potential Vcp is applied, through the capacitors C.

Each of the sense amplifiers 30-0, 30-1, ..., and 30-n comprises P-channel type MOS-FETs Q1 and Q2 ~~which~~ that are connected in series between the bit lines BL0 and BLB0, between the bit lines BL1 and BLB1, ..., and between the bit lines BLn and BLBn and whose gates are connected to the bit lines BLB0, BLB1, ..., BLBn and the bit lines BL0, BL1, ..., and BLn, respectively~~,~~, and N-channel type MOS-FETs Q3 and Q4 ~~which~~ that are connected in series between the bit lines BL0 and BLB0, between the bit lines BL1 and BLB1, ..., and between the bit lines BLn and BLBn and whose gates are connected to the bit lines BLB0, BLB1, ..., BLBn and the bit lines BL0, BL1, ..., and BLn, respectively. Each sense amplifier is configured so that a driving signal from a sense amplifier driver is supplied to the midpoint of connection between the P-channel type MOS-FETs Q1 and Q2 and the midpoint of connection between the N-channel type MOS-FETs Q3 and Q4.

Data read out from the memory cells 10-0, 10-1, ..., and 10-m, each of which comprises a plurality of memory cells, are transmitted to a read DB (data bus) through the sense amplifiers 30-0, 30-1, ..., and 30-n and read gates 40-0, 40-1, ..., and 40-n. Data from a write DB (data bus) are transmitted to and written in the memory cells 10-0, 10-1, ..., and 10-m through write gates 50-0, 50-1, ..., and 50-n and the sense amplifiers 30-0, 30-1, ..., and 30-n.

A D-RAM of the prior art shown in FIG. 3 comprises the D-RAM shown in FIG. 1, and additional read gates 41-0, 41-1, ..., and 41-n ~~which~~ that are provided for the sense amplifiers 30-0, 30-1, ..., and 30-n, respectively. When a transfer gate 20 is on, data read out from the memory cells 10-0, 10-1, ..., and 10-m, each of which comprises a plurality of memory cells, are transmitted to the read DB (data bus) through the sense amplifiers 30-0, 30-1, ..., and 30-n, the transfer gate 20, D latches 60-0, 60-1, ..., and 60-n and the read gates 41-0, 41-1, ..., and 41-n. When the transfer gate 20 is off, the memory device shown in FIG. 3 operates in the same manner as the memory device shown in FIG. 1. The other configuration of the memory device is the same as that of the memory device shown in FIG. 1.

The D-RAM of the prior art shown in FIG. 3 has the following problem. Since data read out from the memory cells 10-0, 10-1, ..., and 10-m pass through the sense amplifiers 30-0, 30-1, ..., and 30-n when the data are transmitted to the D latches 60-0, 60-1, ..., and 60-n, this makes it impossible to make access to the sense amplifiers 30-0, 30-1, ..., and 30-n during the passage of the data~~,~~ or the read data overwrite data of the sense amplifiers 30-0, 30-1, ..., and 30-n.

The above-mentioned D-RAM has a problem of a long access time to a row line. This results from the fact that data of the memory cells of the D-RAM must be amplified and latched by the

sense amplifiers before the data are read out. This is a fundamental problem of the D-RAM.

In order to solve the above-mentioned problems, a plurality of D-RAMs or a D-RAM having a bank structure is used so that the D-RAM operates using banks. More specifically, when access to a bank is being made, another bank is activated to previously enter a ready state so that data are read out consecutively. This is called interleaving. This allows apparently hiding the setup time (tRCD) and the reset time (tPR) required for the D-RAM.

It is possible that a plurality of D-RAMs or the D-RAM having the bank structure is used in order that the D-RAM having a conventional configuration may realize the operation using banks. When a plurality of D-RAMs is used, each D-RAM is not good in area efficiency, but each D-RAM is not limited in operation. On the other hand, the D-RAM having the bank structure is good in area efficiency, because a part of a circuit is common among banks, whereas each bank is partly limited in operation.

The D-RAM has the properties that its larger storage capacity yields its higher area efficiency, while its smaller storage capacity yields its lower area efficiency, similarly to other types of memories. A D-RAM having a multibank structure causes a reduction in area efficiency. Assume that a mixed D-RAM comprises banks of varying minimum units (i.e., blocks), e.g., a 2-Mbit block, a 1-Mbit block, and a 512-Kbit block. If a 4-Mbit D-RAM is manufactured without consideration of the bank structure, the decreasing order of area efficiency, from highest to lowest, is the 2-Mbit block, the 1-Mbit block, and the 512-Kbit block. When a 4-Mbit D-RAM is manufactured in consideration of the bank structure, the D-RAM can be, however, occupied by up to two banks each having the 2-Mbit block, up to

four banks each having the 1-Mbit block, or up to eight banks each having the 512-Kbit block. Even if a D-RAM comprises two banks each having the 1-Mbit or 512-Kbit block, the area efficiency of the D-RAM is not different from that of a D-RAM comprising four banks each having the 1-Mbit block or eight banks each having the 512-Kbit block.

However, a D-RAM having a larger capacity than the ~~a~~ necessary capacity, if a small-capacity D-RAM is used, must be used in order that the D-RAM may operate using banks. In terms of area efficiency, the reason is that the size of the block that is the minimum unit of the bank is large. For example, when a user wants to use a 1-Mbit D-RAM in the form of two banks, a D-RAM of at least 2 Mbits must be used to obtain a D-RAM having a two-bank structure, provided that one block equals 1 Mbit.

The above-mentioned D-RAM adopts a bank method in order to apparently hide the access time to a row line requiring consecutive data.

However, the bank method has to be provided with a D-RAM macro (which refers to a group of circuits having the functions of a D-RAM), and therefore the method is often disadvantageous in area to an application that needs only a small capacity.

A RAM having a capacity of at least 2 Mbits or more must be packaged to employ a bank structure for, for example, an application that requires a RAM having a capacity of only 1 Mbit, if a macro size that can be provided is 1 Mbit and the use of a plural-bank structure is demanded.

The invention is designed to overcome the foregoing problems. It is an object of the invention to provide a memory device which can minimize a reduction in area efficiency, even when the memory device has a small storage capacity, and which can hide the access time to a row line.

SUMMARY OF THE INVENTION

According to a first aspect of the invention, there is provided a memory device which comprises: a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines; a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and a read gate and a write gate ~~which~~ that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, wherein the memory device is controlled so that read data ~~is~~ are read out successively~~,~~ when a word line to be activated~~,~~ of the plurality of word lines is switched to another word line to be activated.

According to the first aspect of the invention, a plurality of memory cells is arranged in a matrix in such a manner that each memory cell is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines~~,~~, a plurality of sense amplifiers capable of read and write operations independently of one another is disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines~~,~~, a read gate and a write gate are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines~~,~~, and the memory device is controlled so that read data ~~is~~ are read out successively~~,~~ when a word line to be activated~~,~~ of the plurality of word lines is switched to another word line to be activated.

According to a second aspect of the invention, there is provided the memory device of the first aspect which comprises a plurality of read gates and a plurality of write gates ~~which~~ that are separately connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to a third aspect of the invention, there is provided the memory device of the first aspect which comprises a common read gate and a common write gate ~~which~~ that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to fourth, fifth and sixth aspects of the invention, there are provided the memories of the first, second and third aspects, wherein each of the plurality of memory cells comprises a dynamic RAM.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a conventional D-RAM;

FIG. 2 is a circuit diagram specifically showing some of circuits shown in FIG. 1;

FIG. 3 is a block diagram showing another conventional D-RAM;

FIG. 4 is a block diagram showing an example of a memory device according to an embodiment of the invention;

FIG. 5 is a timing chart showing waveforms for use in the description of operation of the memory device shown in FIG. 4;

FIG. 6 is a block diagram showing another example of the memory device according to the embodiment of the invention;

FIG. 7 is a timing chart showing waveforms for use in the description of operation of the memory device shown in FIG. 6; and

FIG. 8 is a timing chart showing waveforms for use in the description of operation of the memory devices shown in FIGS. 4 and 6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An example of a memory device (a D-RAM) according to an embodiment of the invention will be described below with reference to FIG. 4. Memory cells 10-0, 10-1, ..., and 10-n each comprise a plurality of memory cells, each of which is connected to ~~an~~ the intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines, similarly to the memory cells described with reference to FIG. 2.

More specifically, the D-RAM has plural, (n+1) pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; plural, (m+1) word lines WL0, WL1, ..., and WLm which intersect the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; a matrix of a plurality of D-RAM memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n}, each of which is connected to an intersection of each bit line and each word line; and a plurality of sense amplifiers 30A-0, 30A-1, ..., and 30A-n, and 30B-0, 30B-1, ..., and 30B-n capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the memory cells 10-0, 10-1, ..., and 10-n, each of which comprises a plurality of memory cells, through the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn~~,~~ via transfer gates 20A and 20B ~~which~~ that are turned on and off in accordance with gate signals TG0 and TG1, respectively.

The configuration of the sense amplifiers 30A-0, 30A-1, ..., and 30A-n, and 30B-0, 30B-1, ..., and 30B-n is the same as that of the sense amplifiers described above with reference to FIG. 2.

Each of the memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n} comprises, for example, an N-channel (or P-channel) type MOS-FET Q, which functions as a switching transistor, and a capacitor C connected in series with the MOS-FET Q.

The drains of the MOS-FETs Q of the memory cells MC0-0, MC2-0, MC4-0, ... of the memory cell 10-0, the memory cells MC0-1, MC2-1, MC4-1, ... of the memory cell 10-1, ..., and the memory cells MC0-n, MC2-n, MC4-n, ... of the memory cell 10-n are connected to the bit lines BL0, BL1, BL2, ..., and BLn, the gates thereof are connected to the word lines WL0, WL2, WL4, ..., and the sources thereof are connected to cell plate potential lines VL to which a common cell plate potential Vcp is applied, through the capacitors C.

The drains of the MOS-FETs Q of the memory cells MC1-0, MC3-0, MC5-0, ... of the memory cell 10-0, the memory cells MC1-1, MC3-1, MC5-1, ... of the memory cell 10-1, ..., and the memory cells MC1-n, MC3-n, MC5-n, ... of the memory cell 10-n are connected to the bit lines BLB0, BLB1, BLB2, ..., and BLBn, the gates thereof are connected to the word lines WL1, WL3, WL5, ..., and the sources thereof are connected to the cell plate potential lines VL to which the common cell plate potential Vcp is applied, through the capacitors C.

Read gates 40A-0, 40A-1, ..., and 40A-n and write gates 50A-0, 50A-1, ..., and 50A-n are connected to the sense amplifiers 30A-0, 30A-1, ..., and 30A-n, respectively.

Read gates 40B-0, 40B-1, ..., and 40B-n and write gates 50B-0, 50B-1, ..., and 50B-n are connected to the sense amplifiers 30B-0, 30B-1, ..., and 30B-n, respectively.

Data read out from the memory cells 10-0, 10-1, ..., and 10-m are transmitted to a read DB (data bus) through the transfer gate 20A, which is turned on in accordance with the gate control signal TG0, the sense amplifiers 30A-0, 30A-1, ..., and 30A-n and the read gates 40A-0, 40A-1, ..., and 40A-n, or through the transfer gate 20B, which is turned on in accordance with the gate control signal TG1, the sense amplifiers 30B-0, 30B-1, ..., and 30B-n and the read gates 40B-0, 40B-1, ..., and 40B-n.

Data from a write DB (data bus) are transmitted to and written in the memory cells 10-0, 10-1, ..., and 10-n through the write gates 50A-0, 50A-1, ..., and 50A-n, the sense amplifiers 30A-0, 30A-1, ..., and 30A-n and the transfer gate 20A turned on in accordance with the gate control signal TG0, or through the write gates 50B-0, 50B-1, ..., and 50B-n, the sense amplifiers 30B-0, 30B-1, ..., and 30B-n and the transfer gate 20B turned on in accordance with the control signal TG1.

Next, the operation of the memory device shown in FIG. 4 will be described with reference to a timing chart shown in FIG. 5. In FIG. 5, CLK represents a clock waveform. Command represents a command from a microcomputer (not shown) which controls the memory device shown in FIG. 3. Address represents row and column address signals from the microcomputer. WL0 and WL1 represent the respective high and low voltages of the word lines WL0 and WL1, respectively. SA0_0, SA0_1, ..., and SA0_n represent the respective voltages of the sense amplifiers 30A-0, 30A-1, ..., and 30A-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively. SA1_0, SA1_1, ..., and SA1_n represent the respective voltages of the

sense amplifiers 30B-0, 30B-1, ..., and 30B-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively.

Data Out represents output data outputted to the read data bus through the read gates. Data In represents input data supplied from the write data bus to the write gates. TGSel represents a gate select signal indicative of either the transfer gate 20A or 20B, from the microcomputer. TG0 and TG1 represent the control signals supplied to the transfer gates 20A and 20B, respectively.

The command Command first indicates ACT to a row address RA0 so as to activate the row address RA0, thus the word line WL0 first changes from low level to high level, and thus the command Command changes to Read so as to read column addresses CA00 and CA01. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the sense amplifiers 30A-0 and 30A-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Then, the sense amplifiers 30A-0 and 30A-1 output the amplified data is transmitted as output data Q00 and Q01 to the read data bus through the read gates 40A-0 and 40A-1, respectively.

The command Command then indicates ACT so as to activate a row address RA1, and thus the word line WL1 first changes from low level to high level so as to read out data of the memory cells. Then, the data are amplified, and thereafter the command Command changes to Read so as to read column addresses CA10 and CA11. After that, the gate select signal TGSel changes to TG1 so as to change the gate signal TG1 from low level to high level, and thus the transfer gate 20B is turned on so as to allow the sense amplifiers 30B-0 and 30B-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Then,

the sense amplifiers 30B-0 and 30B-1 output the amplified data as output data Q10 and Q11 to the read data bus through the read gates 40B-0 and 40B-1, respectively.

The command Command changes to Write, thus the column addresses CA00 and CA01 are read, and data D00 and D01 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30A-0 and 30A-1 through the write gates 50A-0 and 50A-1, respectively. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30A-0 and 30A-1, respectively.

In a state in which the command Command remains Write, the column addresses CA10 and CA11 are read, and data D10 and D11 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30B-0 and 30B-1 through the write gates 50B-0 and 50B-1, respectively. After that, the gate select signal TGSel changes to TG1 so as to change the gate signal TG1 from low level to high level, and thus the transfer gate 20B is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30B-0 and 30B-1, respectively.

After that, the command Command changes to PRE (precharge) so as to precharge the bit lines BL1 and BLB1 of the row address RA1, and thus an equal constant voltage is applied to the bit lines BL1 and BLB1.

Another example of the memory device according to the embodiment of the invention will be described below with reference to FIG. 6. In FIG. 6, the parts corresponding to the parts shown in FIG. 4 are indicated by the same reference numerals and characters, and the description of these parts is

omitted to avoid repetition. Similarly to the memory device shown in FIG. 4, the memory device shown in FIG. 6 has plural, (n+1) pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn~~;~~ ~~plural~~, (m+1) word lines WL0, WL1, ..., and WLm which intersect the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn; a matrix of a plurality of D-RAM memory cells 10-0 {MC0-0, MC1-0, MC2-0, ..., MC(m-1)-0, and MCm-0}, 10-1 {MC0-1, MC1-1, MC2-1, ..., MC(m-1)-1, and MCm-1}, ..., and 10-n {MC0-n, MC1-n, MC2-n, ..., MC(m-1)-n, and MCm-n}, each of which is connected to an intersection of each bit line and each word line; and a plurality of sense amplifiers 30A-0, 30A-1, ..., and 30A-n, and 30B-0, 30B-1, ..., and 30B-n capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the memory cells 10-0, 10-1, ..., and 10-n, each of which comprises a plurality of memory cells, through the bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn~~,~~ via transfer gates 20A and 20B ~~which~~ that are turned on and off in accordance with gate signals TG0 and TG1, respectively.

In this example, common read gates 40-0, 40-1, ..., and 40-n and common write gates 50-0, 50-1, ..., and 50-n are connected in parallel with the sense amplifiers 30A-0 and 30B-0, 30A-1 and 30B-1, ..., and 30A-n and 30B-n through transfer gates 20C and 20D ~~which~~ that are turned on and off in accordance with gate signals TGA0 and TGA1, respectively. The other configuration of the memory device shown in FIG. 6 is the same as that of the memory device shown in FIG. 4.

Next, the operation of the memory device shown in FIG. 6 will be described with reference to a timing chart shown in FIG. 7. In FIG. 7, the parts corresponding to the parts shown in FIG. 5 are indicated by the same reference numerals and characters, and thus the description of these parts is omitted

to avoid repetition. TGASel represents a gate select signal indicative of either the transfer gate 20C or 20D.

The command Command first indicates ACT so as to activate a row address RA0~~,~~; thus, the word line WL0 first changes from low level to high level, ~~thus~~ the command Command changes to Read, and ~~thus~~ the gate select signal TGSel changes to TG0 so as to read column addresses CA00 and CA01. After that, the gate signal TG0 changes from low level to high level, and thus the transfer gate 20A is turned on so as to allow the sense amplifiers 30A-0 and 30A-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Thereafter, the gate select signal TGASel changes to TGA0 so as to change the gate signal TGA0 from low level to high level, and thus the transfer gate 20C is turned on. Then, the sense amplifiers 30A-0 and 30A-1 output the amplified data as output data Q00 and Q01 to the read data bus through the read gates 40-0 and 40-1, respectively.

The command Command then indicates ACT so as to activate a row address RA1~~,~~; thus, the word line WL1 first changes from low level to high level, ~~thus~~ the command Command changes to Read, and ~~thus~~ the gate select signal TGSel changes to TG1 so as to read column addresses CA10 and CA11. After that, the gate signal TG1 changes from low level to high level, and thus the transfer gate 20B is turned on so as to allow the sense amplifiers 30B-0 and 30B-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Thereafter, the gate select signal TGASel changes to TGA1 so as to change the gate signal TGA1 from low level to high level, and thus the transfer gate 20D is turned on. Then, the sense amplifiers 30B-0 and 30B-1 output the amplified data as output data Q10 and Q11 to the read data bus through the read gates 40-0 and 40-1, respectively.

The command Command changes to Write, and thus the column addresses CA00 and CA01 are read. The gate select signal TGASel first indicates TGA0 so as to change the gate signal TGA0 from low level to high level, and thus the transfer gate 20C is turned on. Data D00 and D01 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30A-0 and 30A-1 through the write gates 50-0 and 50-1, respectively. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30A-0 and 30A-1, respectively.

In a state in which the command Command remains Write, the column addresses CA10 and CA11 are read. The gate select signal TGASel first indicates TGA1 so as to change the gate signal TGA1 from low level to high level, and thus the transfer gate 20D is turned on. Data D10 and D11 from the write data bus are written in and inverted, amplified and latched by the sense amplifiers 30B-0 and 30B-1 through the write gates 50-0 and 50-1, respectively. After that, the gate select signal TGSel changes to TG1 so as to change the gate signal TG1 from low level to high level, and thus the transfer gate 20B is turned on so as to allow the memory cells 10-0 and 10-1 to store the data of the sense amplifiers 30B-0 and 30B-1, respectively.

After that, the command Command changes to PRE (precharge) so as to precharge the bit lines BL1 and BLB1 of the row address RA1, and thus an equal constant voltage is applied to the bit lines BL1 and BLB1.

Incidentally, a D-RAM is characterized by ~~that~~ the activation of an address of a row line allows a sense amplifier to read out a few thousands of bits of data, which is then selectively read out by controlling an address of a column line.

Generally, the operation of activating the address of the row line so as to prepare data for ~~the~~ reading is very slow, which is a drawback of the D-RAM. The technique for eliminating the drawback is interleaving using a bank structure, which is described in the section "Description of the Related Art". More specifically, when data of a bank ~~is~~ are being read out, data of another bank ~~is~~ are prepared, and thus the latter data can be read out in succession to the former data immediately after the end of reading ~~of~~ the former data. However, the interleaving requires a plurality of banks, and therefore causes a reduction in area efficiency in the case of a small-capacity memory device.

However, the memories shown in FIGS. 4 and 6 are each provided with a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with a plurality of memory cells, each of which is connected to each of the pairs of bit lines, through the pairs of bit lines, and the memories are controlled so that read data may be read out successively~~,~~ when a word line to be activated~~,~~ of a plurality of word lines is switched to another word line to be activated. Therefore, the above-described memories can minimize ~~a~~ the reduction in area efficiency even when the memories have a small capacity, and the memories also enable operation equivalent to the interleaving performed by a memory device having ~~the~~ a bank structure (see FIG. 8).

In FIG. 8, the parts corresponding to the parts shown in FIGS. 5 and 7 are indicated by the same reference numerals and characters, and thus the description of these parts is omitted to avoid repetition.

The memories shown in FIGS. 4 and 6 are each provided with a plurality of sense amplifiers capable of read and write

operations independently of one another, which are disconnectedly connected in parallel with a plurality of memory cells, each of which is connected to each of the pairs of bit lines, through the pairs of bit lines~~;~~, and read gates and write gates ~~which~~ that are connected to a plurality of sense amplifiers connected to a plurality of memory cells. Therefore, when one sense amplifier is being used to write and read data in/from a memory cell, another sense amplifier can be used to sense a subsequent row address, so that an erroneous hit of a page can be prevented.

When one sense amplifier is being used to write and read data in/from a memory cell, another sense amplifier may be used as a static RAM (an S-RAM).

For example, when 2-Mbit blocks are used to manufacture a D-RAM having a storage capacity of 4 Mbits, the D-RAM has a structure of only up to two banks. Therefore, 1-Mbit or 512-Kbit blocks must be used in order that a D-RAM may comprise four banks. However, as described above, the adoption of a system comprising a plurality of sense amplifiers permits manufacturing a D-RAM having functions substantially equivalent to functions of a D-RAM comprising four banks using 2-Mbit blocks. Accordingly, although a larger number of additional sense amplifiers yield a lower area efficiency of a memory device, the memory device is greatly improved in area efficiency as compared to a memory device using 1-Mbit or 512-Kbit blocks.

According to a first aspect of the invention, a memory device comprises: a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines; a plurality of sense amplifiers capable of read and write operations independently of one another, which are

disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and a read gate and a write gate ~~which~~ that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, wherein the memory device is controlled so that read data ~~is~~ are read out successively, when a word line to be activated, of the plurality of word lines is switched to another word line to be activated. Therefore, the memory device can minimize a reduction in area efficiency, even when the memory device has a small storage capacity, ~~can~~ realize operation equivalent to interleaving using the bank structure, ~~can~~ hide the access time to a row line, and can use as an S-RAM any one of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to a second aspect of the invention, the memory device of the first aspect comprises a plurality of read gates and a plurality of write gates ~~which~~ that are separately connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines. Therefore, the memory device can minimize ~~a~~ the reduction in area efficiency even when the memory device has a small storage capacity, ~~can~~ realize operation equivalent to interleaving using the bank structure, ~~can~~ hide the access time to a row line, and ~~can~~ use as an S-RAM any one of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

According to a third aspect of the invention, the memory device of the first aspect comprises a common read gate and a common write gate ~~which~~ that are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines. Therefore, the memory device can minimize a reduction in area efficiency, even when the memory device has a small storage capacity, ~~can~~ realize operation equivalent to

interleaving using the bank structure, ~~can~~ hide the access time to a row line, ~~can~~ use as an S-RAM any one of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, and ~~can~~ have a smaller number of read gates and write gates connected to the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

In the memories of the first, second and third aspects, each of the plurality of memory cells comprises a dynamic RAM.

Having described preferred embodiments of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments and that various changes and modifications could be effected therein by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended claims.

ABSTRACT OF THE DISCLOSURE

Disclosed is a memory device which can minimize a reduction in area efficiency even when the memory device has a small storage capacity and which can hide the access time to a row line. The memory device comprises: a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines; a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and a read gate and a write gate which are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines, wherein the memory device is controlled so that read data ~~is~~ are read out successively~~,~~ when a word line to be activated~~,~~ of the plurality of word lines is switched to another word line to be activated.

ATTACHMENT E

Atty Docket No.: SON-2357

Inventor: Tomofumi Arakawa

Application No.: 10/060,226 **Filing Date:** February 1, 2002
Title: MEMORY DEVICE

Documents Filed:
Request to Withdraw Erroneous holding of abandonment

Via:
Sender's Initials: RPK/sjm **Date:** October 21, 2003

SON-2352

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Tomofumi Arakawa

Confirmation No. 8077

Application No.: 10/060,226

Group Art Unit: 2818

Filed: February 1, 2002

Examiner: Huan Hoang

For: MEMORY DEVICE

REQUEST TO WITHDRAW ERRONEOUS HOLDING OF ABANDONMENT

Commissioner for Patents
Mail Stop Issue Fee
P.O. Box 1450
Alexandria, Va 22313-1450

Sir:

The Applicant, through its attorneys, hereby requests withdrawal of the erroneous Notice of Abandonment mailed in the above-identified application on September 24, 2003. No fee is believed required to support this request. However, if a fee is required, the Commissioner is hereby authorized to charge the fee to Deposit Account # 18-0013.

In the Notice of Abandonment of September 24, 2003, the Examiner alleged that Applicant failed to timely respond to the Notice to File Corrected Application Papers Mailed on May 2, 2003. This is incorrect as evidenced by the enclosed copy of the Response to Notice to File Corrected Application Papers timely filed on June 2, 2003, together with a copy of the postcard receipt stamped "June 2, 2003" by the U.S. Patent Office. This stamped postcard receipt is competent evidence that the Response was timely filed. Thus the Notice of Abandonment is in error.

Applicant respectfully requests an official withdrawal of the Notice of Abandonment and a prompt issuance of the allowed application.

Prompt action on this matter is respectfully solicited.

Respectfully submitted,

Dated: October 21, 2003

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